EE 3610 Digital Systems

Lab 0

Title: Using ISE to program the Spartan 3E Starter Board.

Objective: The student will use ISE to synthesize a simple circuit, download it and test it on the Spartan 3E Starter Board.

Equipment: Spartan 3E Starter Board with Power Supply and USB cable
Computer with ISE WebPack installed.

Overview: In this exercise, you will design a 2-input logic gate, reduce it to a "bit file" and download that file onto the Spartan 3E Starter Board (supplied).

Software: You will be using an application called ISE to design your circuits this semester. This application is available in the lab (Room 418), but it will be to your advantage to download it on your own computer if possible. The application is enormous, so make sure you have at least 20 GB free on your hard disk before you start. You can find the download page for version 13.4 (the same as in the lab) at:

http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/v13_4.html

You will be directed to create an account, and after the download is complete you will need to request a Webpack license. (The Webpack license is free and never expires, but it does have limitations). This process takes time, so it is recommended that you start several days before lab.

Preliminary: Other than installing the ISE software, there is no advanced preparation required for this lab.

Procedure: Start ISE and wait. This is a good time to get a cup of coffee or change the oil in your car. Alternatively, you might read a short novel. You probably don't have time for War and Peace, but you might finish The Hitchhiker's Guide to the Galaxy before ISE comes up.

Create a new project. Select the "New Project" button as shown in Figure 1.

You will now need to create a project folder. On the lab machines, most of the disk is read-only, so you will have to put it in your folder under C:\Users. (Or, you may use your memory stick). Type the folder's name (or browse) in the location box to select the desired folder (Figure 2). Then give the project a name in the name box. This will create the project file and, if necessary, the folder to put it in. (Note, you do not need to type in the "Working Directory" box – it will be filled automatically.)

Double check to make sure the top level source type is HDL.

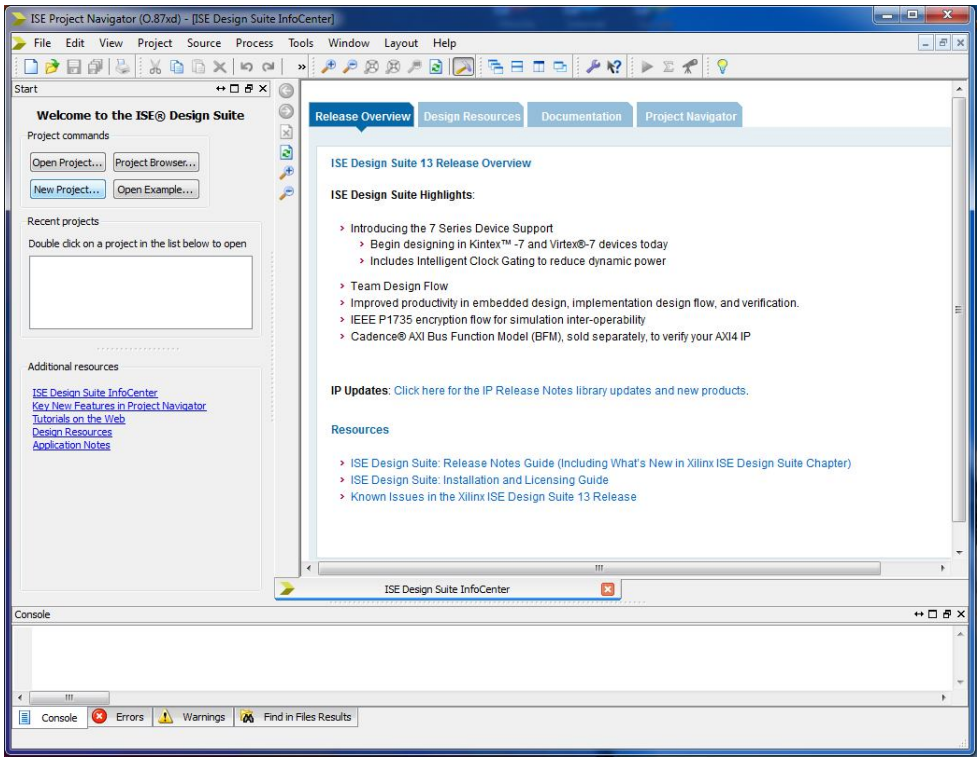


Figure 1.

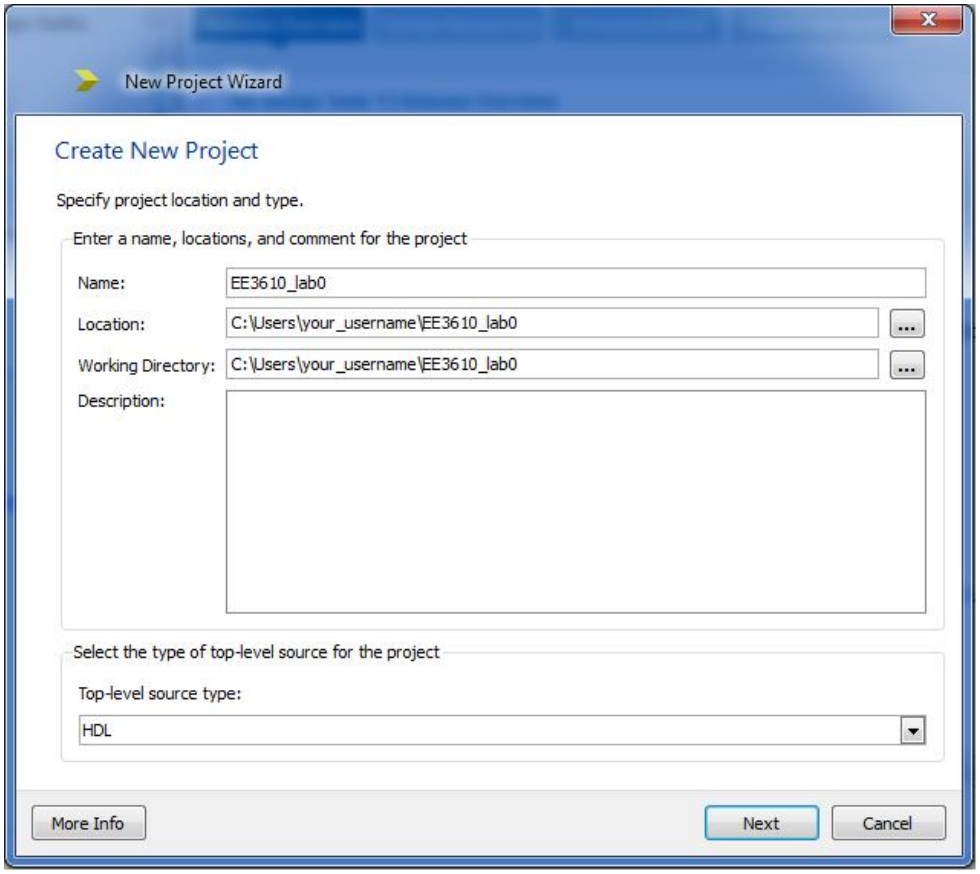


Figure 2.

Press “Next”. At this point you will need to specify the hardware to be used. In this case, select the Spartan 3E Starter Board. (See Figure 3.) (Alternatively, you may also select Spartan3E, XC3S500E and FG320 individually.) Set the preferred language to VHDL (Figure 4).

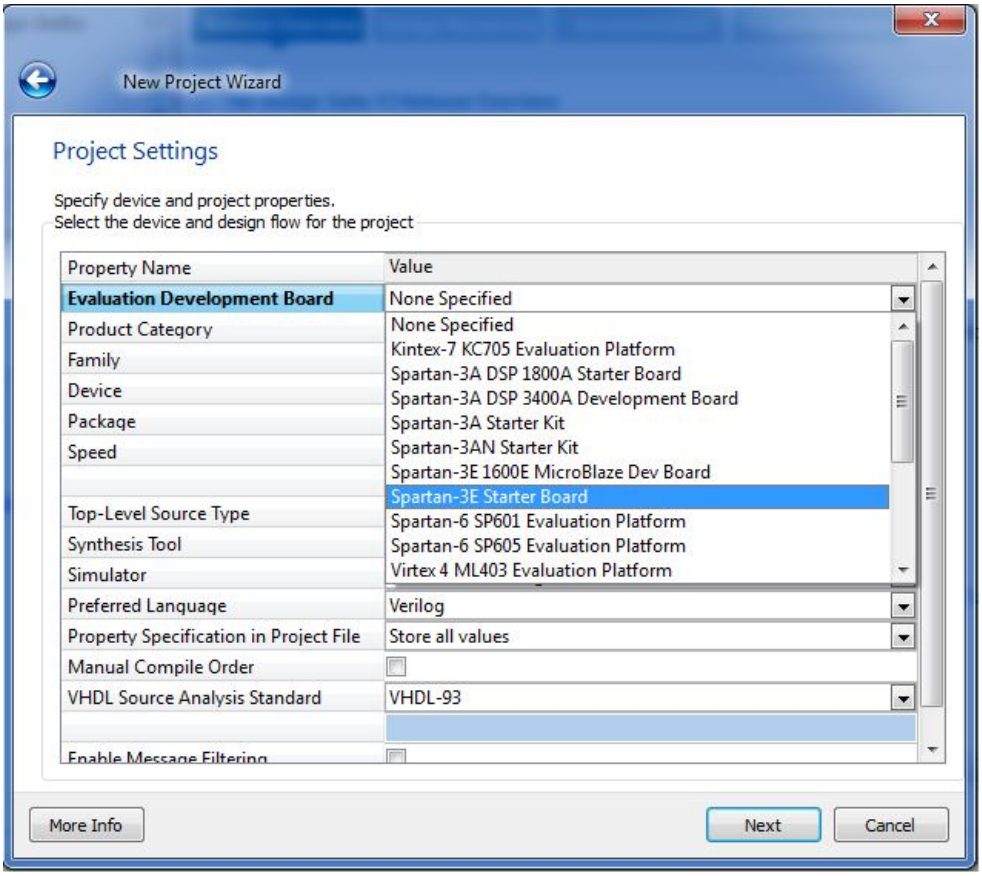


Figure 3.

Once you have the proper configuration, the dialog box should resemble the one in Figure 4. Click “Next”, review the configuration and click “Finish”.

Now your project is configured, but it doesn’t contain any files. Select Project->New Source and create a new VHDL module called top.vhd. When prompted, create 2 inputs called SW0 and SW1 and create one output called LED0. Click “Next” then “Finish”.

Using the editor, complete the skeleton VHDL program by typing:

```
LED0 <= SW0 xor SW1;
```

after the begin keyword. Save top.vhd.

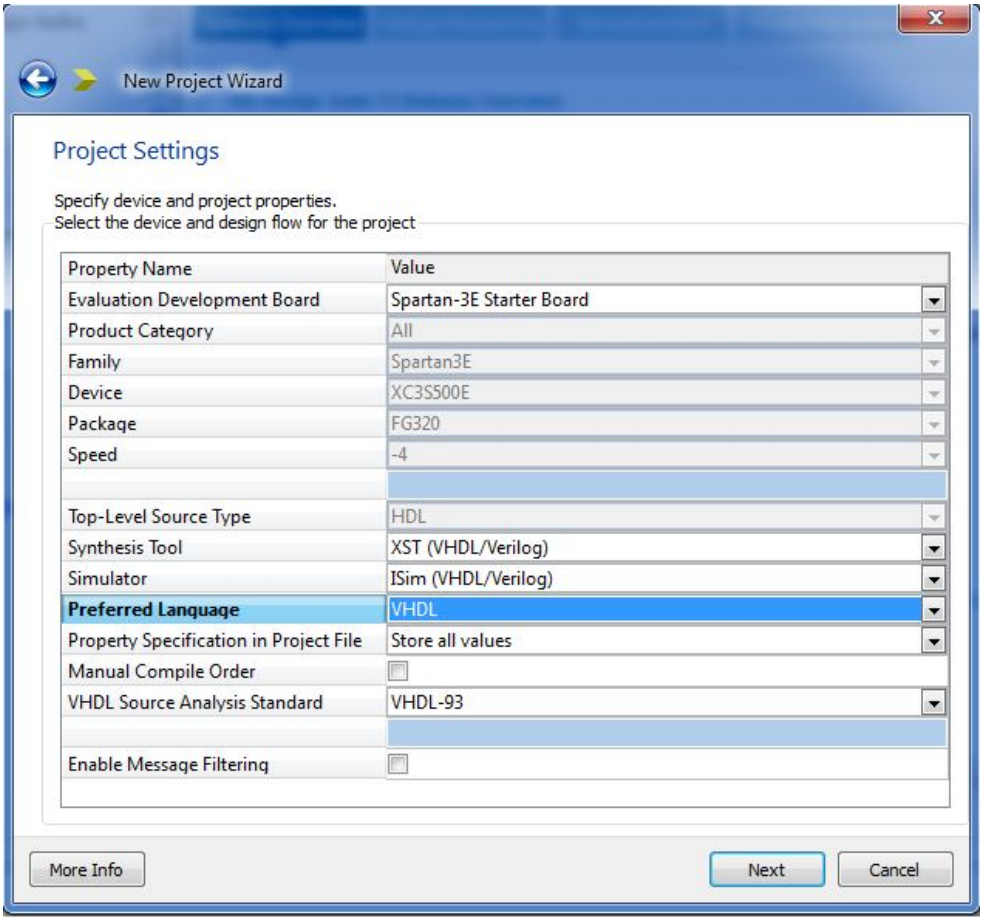


Figure 4.

We need to create a constraints file to bind the inputs and outputs of the top module to actual pins on the FPGA. Select Project->New Source then select implementation constraints file. Give your constraints file a name, click “Next” then “Finish”.

Type the following constraints into your new constraints file:

```
NET "SW0" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW1" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
NET "LED0" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
```

Save the file. Now you are ready to synthesize. Make sure your screen looks something like Figure 5. Make sure the radio button labeled “Implementation” is selected, top.vhd is selected and your constraints file is associated with top.vhd.

Double-click Synthesize – XST. Assuming there are no errors, a green check or a yellow exclamation mark will appear by the selection when synthesis completes.

After synthesis completes, double-click “Implement Design”. This step fits the generic results of the synthesis to the Spartan 3E FPGA.

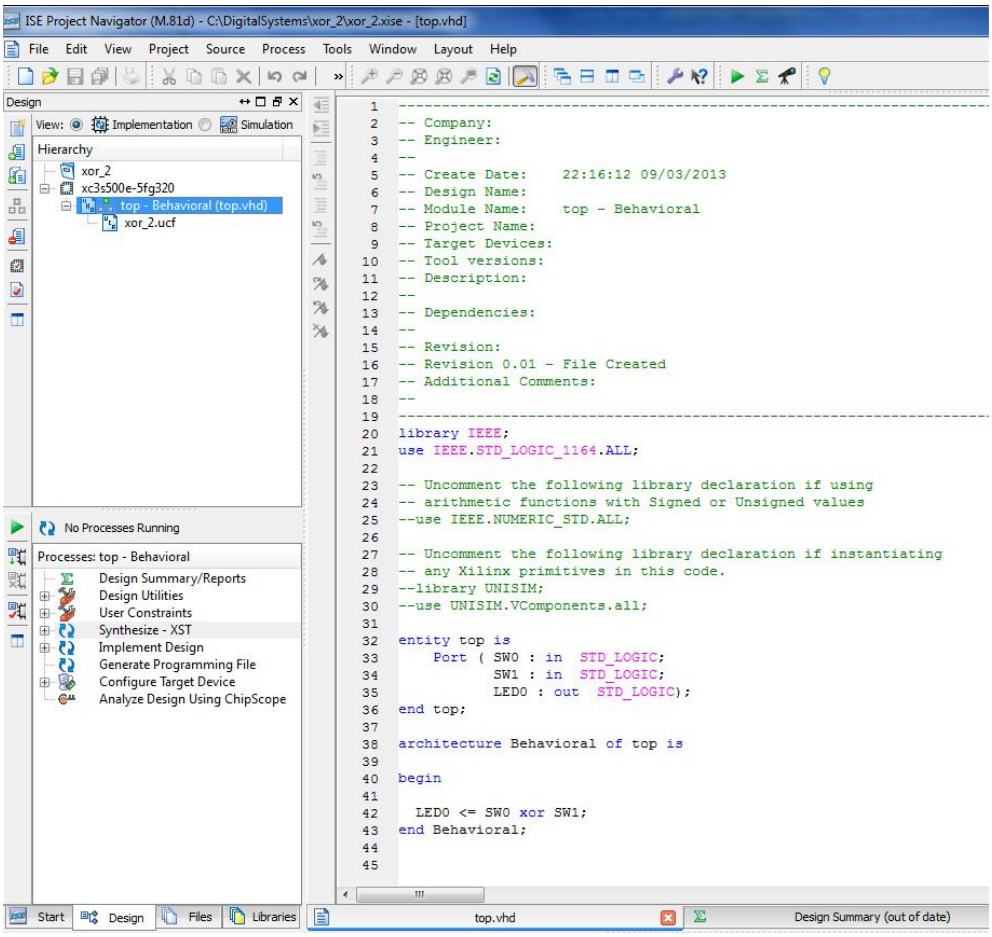
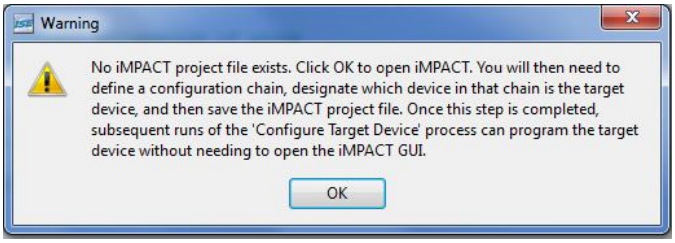


Figure 5

When this process concludes, double-click “Generate Programming File”. This takes your design and reduces it to a “.bit” file that contains the 1’s and 0’s necessary to program the Spartan 3E FPGA.

Using windows (file) explorer, find the project folder and verify that it contains a file called top.bit. This file is the culmination of the entire design effort so far. What remains is to download it to the Spartan 3E FPGA.

The process of downloading the .bit file is surprisingly complicated. Start by connecting the USB cable between your PC and the Spartan board. Then, you must run a program called iMPACT, which you can do by double-clicking “Configure Target Device”. ISE looks for an iMPACT project file, and when it doesn’t find one, you will get the nasti-gram below:



Click “OK” and wait patiently. Eventually, iMPACT will come up. Double-click “Boundary Scan” then right-click in the large white window on the upper right to initialize the scan chain (Figure 6).

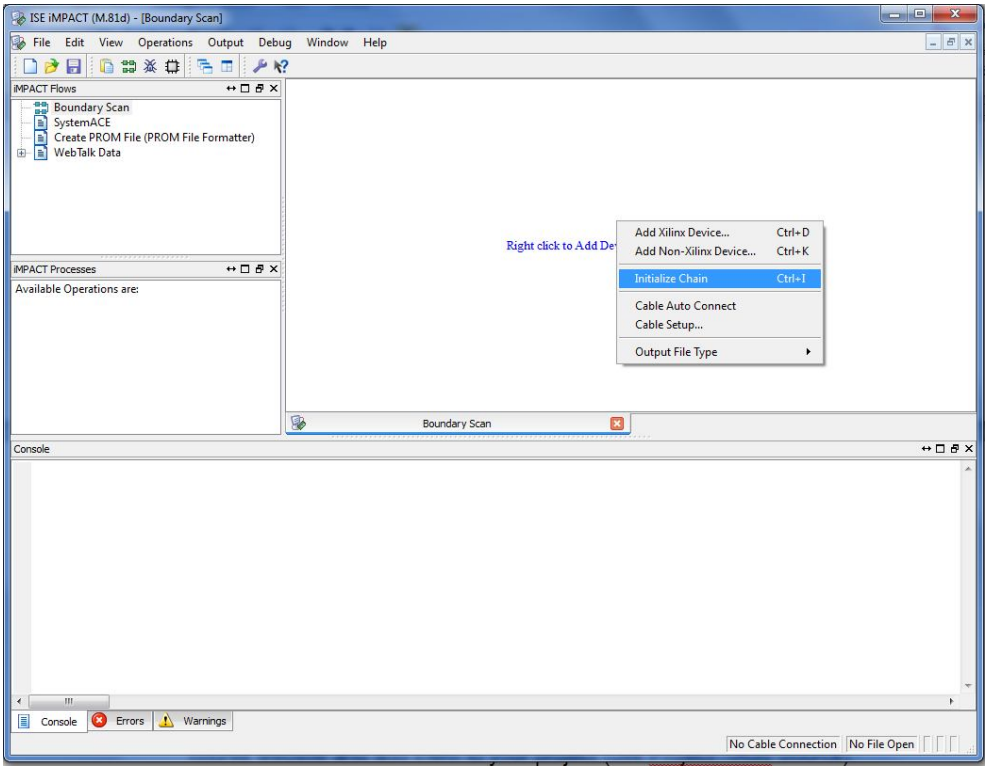


Figure 6

If the initialization of the scan chain succeeds, you should see a screen something like that in Figure 7. If you do not, check your connections, check that the board has power, and check that the driver for the Xilinx USB cable is installed correctly.

Once you have the screen in Figure 7, answer yes to the dialog box to assign configuration files. The first chip to assign is the xc3s500e. Select top.bit for that one and click “Open” (Figure 8). You be asked if you wish to attach a PROM. Answer No.

There are 2 other programmable devices on the Spartan 3E Starter Board (the xcf04s and the xc2c64a). We are not interested in configuring these, so click “Bypass” when prompted for these devices. Also, if a “Device Programming Properties” dialog box appears, simply click OK to continue.

The next step is to identify the xc3s500e as the “Target” device. This is done by right-clicking the xcs500e and selecting “Set Target Device” (Figure 9).

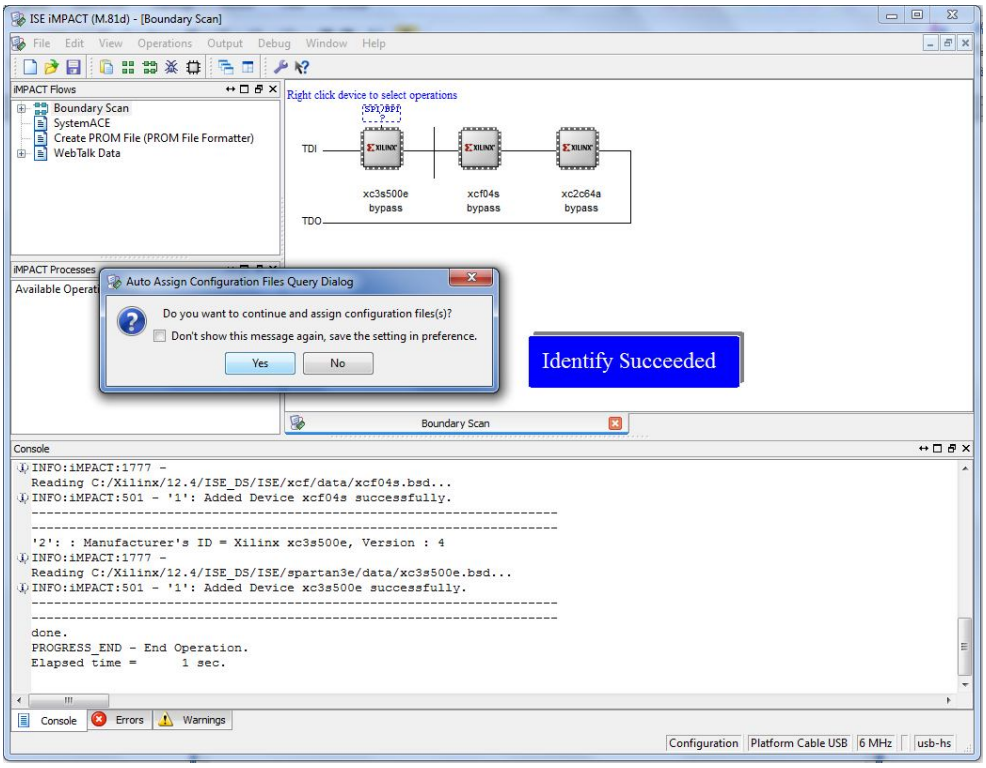


Figure 7

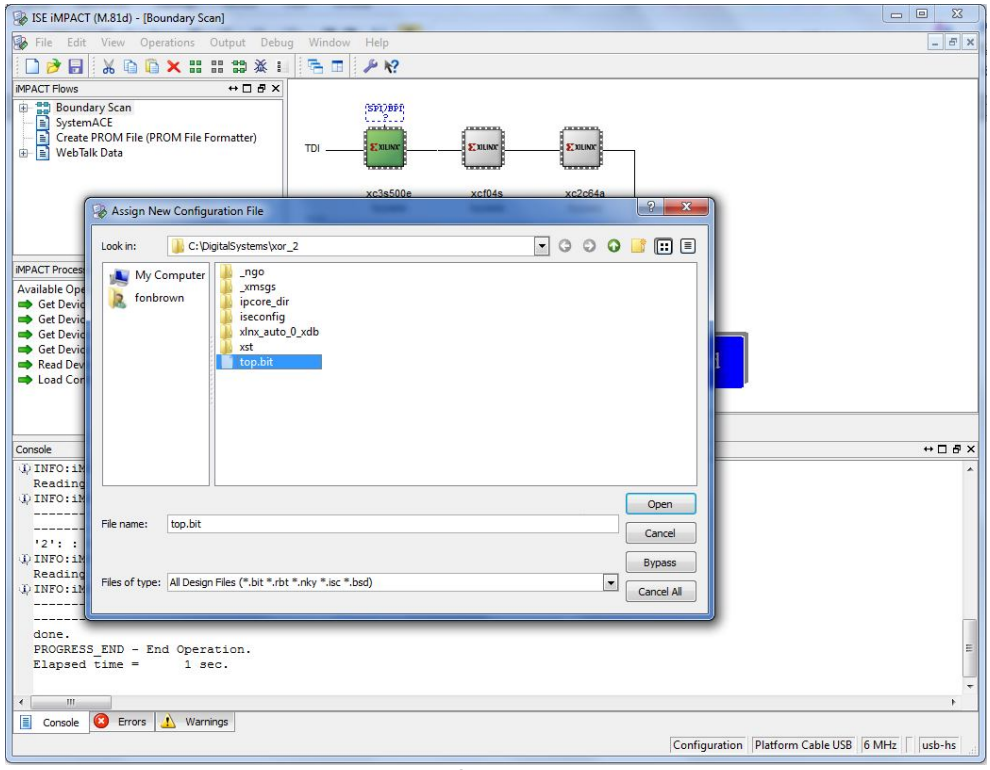


Figure 8

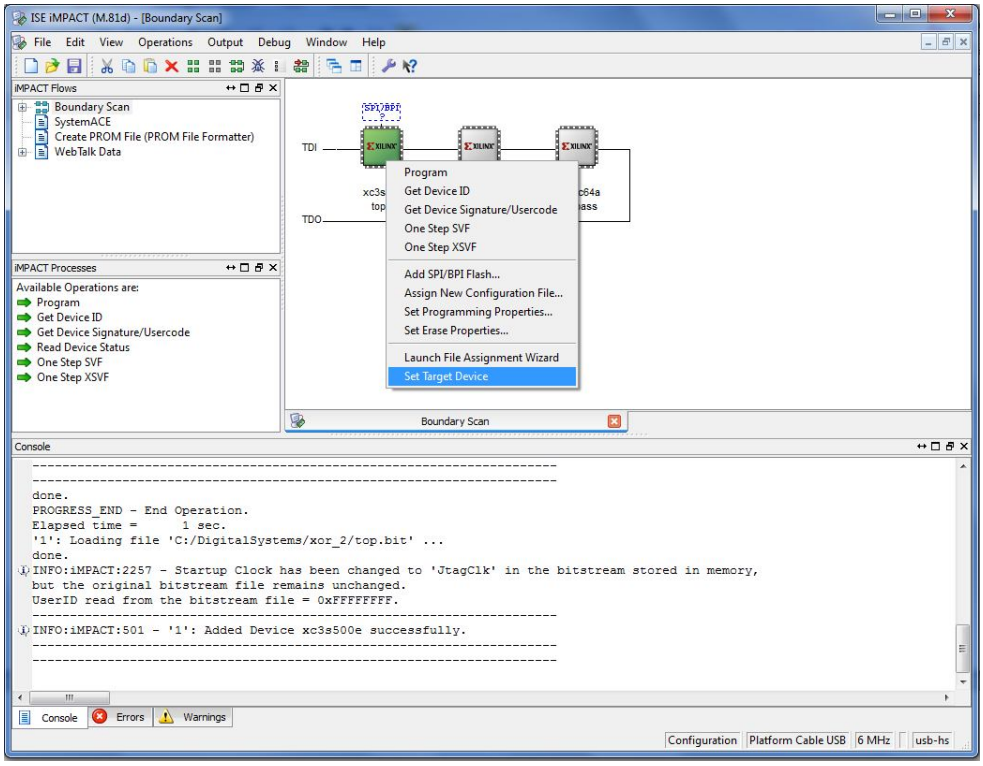


Figure 9

If you are anxious to see the program run, you may now double-click "Program" and download the bit file. If your circuit works, switching SW0 or SW1 on the Spartan Board will toggle LED0.

Still, we have a little more work to do to finish the iMPACT configuration. Select File→Save Project, choose an iMPACT Project File name and save it IN THE SAME FOLDER as your project (This doesn't always happen by default).

Exit IMPACT and return to ISE. Right-click on "Configure Target Device" and select "Process Properties" (Figure 10).

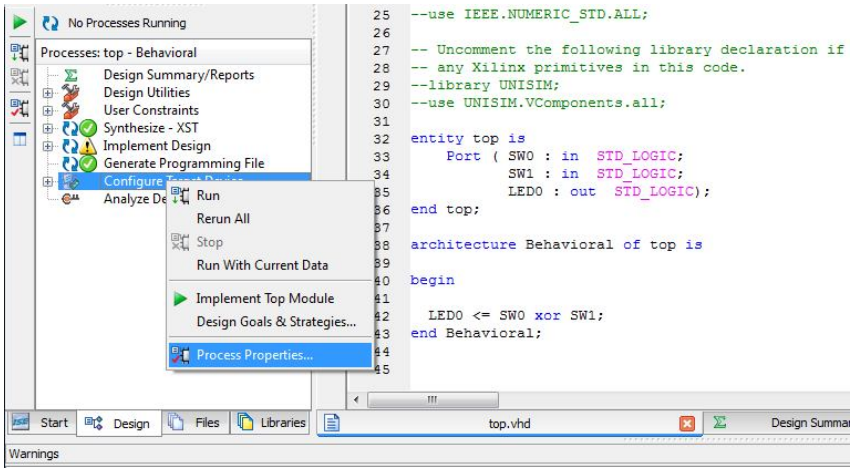


Figure 10

For the property called “iMPACT Project File”, browse to the (.ipf) file you just saved then click OK.

iMPACT should now be completely configured. To test it, change **xor** in top.vhd to **or**:

```
LED0 <= SW0 or SW1;
```

Save top.vhd then double-click “Configure Target Device”. Watch as ISE Synthesizes, Implements, Generates a Programming File and downloads it automatically.

Demonstrate this new program to your lab instructor. This assignment is worth 5 lab points if demonstrated prior to the end of the lab period and 4 points thereafter.